REMARKS

Claims 1-17 are pending in the application of which claims 1 to 12 and 14 have been withdrawn from consideration.

Claim 13 has been amended to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention.

Claim Rejections under 35 U.S.C. §102(b)

Claims 13 and 15 to 17 stand rejected under 35 U.S.C. 102(e) as being anticipated by Higashi et al. (U.S. Publication No. 2003/0102547 A1).

The present invention is an electronic parts packaging structure in which five embodiments are described in the specification. Claims 13 and 15-17 which are currently being prosecuted are directed to the first embodiment as illustrated in Figures 2A-2H. The first embodiment includes, as shown in Figure 2A, a base substrate (24) on which a wiring substrate is prepared. Through-holes (24a) are provided in the base substrate (24) and through-hole plating layers (24b) are connected to a first wiring patterns (28). A first interlayer insulation film (30) is placed on top of the first wiring patterns (28). First via holes (30x) are formed on the first interlayer insulation film (30). A second wiring patterns (28a) is formed on the first interlayer insulation film (30). As shown in Figure 2B, a first resin film (32a) is formed on the second wiring patterns (28a) and the first interlayer insulation film (30). As shown in Figure 2C, a semiconductor chip (20) (electronic parts)is embedded in the first resin film (32a). Connection pads (21a) (connection terminals) are exposed on the element

formation surface of the semiconductor chip (20). As shown in Figure 2D, a second interlayer insulation film (32) is created composed of the first resin film 32a (first insulating film) and a second resin film (32b) (second insulation film). As shown in Figure 2E, via holes (32x) are formed in the second interlayer insulation film (32) on the connection pads (21a) of the semiconductor chip (20) and on the second wiring patterns (28a). As shown in Figure 2G, a third wiring patterns (28b) (upper wiring patterns) are connected to the connection pads (21a) of the semiconductor chip (20) and to the second wiring patterns (28a) through the second via holes (32x), formed on the second interlayer insulation film (32). Finally, an upper semiconductor chip (20x) (upper electronic parts) with bumps (23) which are flip-chip bonded to the connection portions (28z) of the third wiring patterns (28b).

Higashi et al. shows some remarkable similarities with the present invention. These similarities can be most notably seen in Figure 3(c) of Higashi et al. and Figure 2H of the present application. Higashi et al. shows a substrate (20), insulating layers (32a and 32b), semi-conductor chips (12) and a wiring pattern (22a). However, there are some notable differences.

(1) The back side of the electronic part in the present invention is electrically insulated with the wiring pattern of the wiring substrate by the lower portion of the first insulating film. Because the lower portion of the first insulating film functions as the adhesive layer for pasting the electronic part.

However, in Higashi et al., the back side of the electronic part is electrically connected to the wiring pattern of the wiring substrate by a bump formed in the back side of the electronic part. That is, the back side of electronic part does not insulated with the wiring pattern of the wiring substrate.

(2) The electrical path of the present invention as recited in claim 13 differs from that of Higashi et al. That is, in claim 13, the connection pad formed in the upper surface of the electrical part is electrically connected to the wiring pattern of the wiring substrate by only the upper wiring pattern. In claim 13, electrical path has nothing in back side of the electronic part.

However, in Hagashi et al., the back side of the electronic part is electrically connected to the wiring pattern of the wiring substrate by the bump. Hagashi et al. fails to describe that the electrical part is electrically connected to the wiring pattern of the wiring substrate by only upper wiring pattern arranged above the electronic part.

In order to clarify the claimed present invention, claim 13 has further been amended. Specifically, the lower portion of the first insulating film which exists between the back side of the electronic parts and the wiring substrate functions as an adhesive layer for mounting the electronic parts above the wiring substrate. This results in a whole of the back side of the electronics parts being electrically insulated with the wiring substrate.

Therefore, withdrawal of the rejection of claims 13 and 15 to 17 under 35 U.S.C. 102(e) as being anticipated by Higashi et al. (U.S. Publication No. 2003/0102547 A1) is respectfully requested.

Conclusion

In view of the aforementioned amendments and accompanying remarks, claim 13, as amended, is believed to be patentable and in condition for allowance, which action, at an early date, is respectfully requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, the applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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